Application No.: 10/075,591 Docket No.: 500.41141X00

AMENDMENTS TO THE SPECIFICATION

Page 15

Please amend the paragraph beginning on line 3 and bridging page 16, line 9, as follows:

The first half of one horizontal scanning period is a "writing period" of a display signal. At timing (1) in the figure, the gate line 6 and the reset line 10 on a selected pixel line (here, nth line) go high. Because in this embodiment the input ~~FTF~~TFT 1 and the reset TFT 9 are of n-channel, the gate line 6 and the reset line 10 represent an on-state when they are at high level (on high voltage side) and an off-state when they are at low level (on low voltage side). Thus, at this timing, the input TFT 1 and the reset TFT 9 on the selected pixel line are turned on. When the reset TFT 9 turns on, the input/output voltage of the inverter circuit 3 is reset to Vrst, which is applied to one end of the storage capacitor 2, as described in the preceding paragraphs concerning the operation of the inverter circuit 3. At the same time, a predetermined display signal voltage is input to each of the signal lines 7. This display signal voltage is applied to the other end of the storage capacitor 2 through the turned-on input TFT 1. After this, the voltage of the reset line 10 goes low, turning off the reset TFT 9. The above operation writes into each of the storage capacitors 2 on the selected pixel line a signal charge that is required to feed Vrst to the input of the inverter circuit 3 when the above display signal voltage is entered from the signal line 7. If the rise characteristic of the inverter circuit 3 is sufficiently steep, the values of Vrst and Von are very close to each other and can be regarded approximately as the same voltage. That is, when the display signal voltage is applied to the pixel from the signal line 7, the output of the inverter circuit 3 becomes almost Velon, turning

Amd. the OLED 4 on or off. In Fig. 5, the values of Vrst and Von are shown approximately to be the same voltage for the sake of simplicity.